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PATENT RANGE:

1. A kind of Ethernet switching device with share memory structure, which is used to deliver network packet selectively, the said device includes: a memory device which provides accessing network packet, and store network routing data; a memory controller coupled to the said memory device is used to manage and control network packet in the said memory device; a data switching controller coupled to the said memory device is used to control the routing and learning of network packet routing; and two network ports which are coupled to said memory controller and data switching controller.

2. The said Ethernet switching device as claimed in claim 1 in the patent range, in which, the said memory device further includes: a routing table coupled to the said memory controller, which stores the routing table data of the said data switching controller through the said memory controller; and a packet buffer coupled to the said memory controller, which allows packet access of every said network port through the said memory controller.

3. The said Ethernet switching device as claimed in claim 1 or 2 in the patent range, in

which, the said memory controller further includes: an external memory interface coupled to the said memory device, said data switching controller, and every said network port respectively, which is used to control the data access of the said memory device; and a memory manager coupled to every said network port respectively, which manager the said memory device through the said external memory interface.

4. The said Ethernet switching device as claimed in claim 3 in the patent range, in which, the said memory manager further includes: a buffer table records the usage state of the said memory device through every said network port and said external memory interface; and a buffer manager coupled to the said buffer table, which managers the said packet buffer according to the obtained usage state of the said packet buffer.

5. The said Ethernet switching device as claimed in claim 1 or 2 in the patent range, wherein the said data switching controller further includes: a routing controller which is used to select the packet routing of every said network port; and a learning controller which is used to store the packet routing selected by the said routing controller into the routing table of the said memory device through the said memory controller.

6. As the said Ethernet switching device claim 5 in the patent range, wherein the said routing controller should route the corresponding network port selectively according to the destination address of received packet.

7. The said Ethernet switching device as claimed in claim 5 in the patent range, wherein the said learning controller should route the corresponding network port selectively according to the source address of received packet.

8. The said Ethernet switching device as claimed in claim 1 or 2 in the patent range, wherein the said network port further includes: an Ethernet communication protocol controller which mainly accomplishes the function regulated by IEEE 802.3 section 4; and a network packet data access controller which is used to receive and deliver network packet.

9. The said Ethernet switching device as claimed in claim 8 in the patent range, wherein the said Ethernet communication protocol controller further includes: a MII; a reconciliation sub-layer; and a MAC that has receiving and delivering function which are accord with IEEE 802.3 section 4.

10. The said Ethernet switching device as claimed in claim 8th item in patent range, in which, the said network packet data access controller further includes: an RxDMA which is used to receive network packet; and TxDMA which is used to deliver network packet.

11. A kind of Ethernet switching device with share memory structure, which is used to deliver network packet selectively, the said device includes: a routing table; a packet buffer; a share memory access controller coupled to the said routing table and said packet buffer respectively, which has arbitrating, data multiplexing, address, and commands function; a data switching controller coupled to the said share memory access controller, which has initializing, arbitrating, aging routing table, routing and learning function; more than two network ports, and every said network port is coupled to the said share memory access controller and said data switching controller respectively; a buffer manager coupled to every said network port; and a buffer table coupled to said buffer manager; in which, the said routing table stores the routing data of the said data switching controller through the said share memory access controller; the packet buffer accepts packet accessing of every said network port through the said share memory access controller; the said buffer table records the usage state of the said packet buffer through every said network port and share memory access controller; and the said buffer manager managers the said packet buffer according to the obtained usage state of the said packet buffer through every said network port and said share memory access controller.

12. The said Ethernet switching device as claimed in claim 11 in the patent range, wherein the said network port further includes: an Ethernet communication protocol controller which mainly accomplishes the function regulated by IEEE 802.3 section 4; and a network packet data access controller which is used to receive and deliver network packet.

13. The said Ethernet switching device as claimed in claim 12 in the patent range, wherein the said Ethernet communication protocol controller further includes: a MII; a reconciliation sub-layer; and a MAC that has receiving and delivering function which are accord with IEEE 802.3 section 4.

14. The said Ethernet switching device as claimed in claim 12th item in patent range, in which, the said network packet data access controller further includes: an RxDMA

which is used to receive network packet; and TxDMA which is used to deliver network packet.

15. A kind of Ethernet switching device which is used to deliver network packet selectively, the said device includes: multiple MAC which is used to receive and deliver network packet; and a switching controller coupled to every said network port respectively, which has a share memory to control the ports of every MAC.

16. A kind of Ethernet switching buffering management method, the said Ethernet switching includes external memory with routing table, a buffer manager, and several network ports which include RxDMA and TxDMA, and the said buffering management method includes: dividing the said external memory into several blocks, and assigning a buffer ID to every said block to present the relative packet position of external memory; the said buffer manager maintains the linked list of the said buffer ID, and assigns the said buffer ID dynamically to every forward packet; the said buffer manager assigns free buffer ID to said RxDMA; and the said buffer manager withdraws said buffer ID from TxDMA.

17. The said buffering management method as claimed in claim 16 in the patent range further includes: the said RxDMA will need a buffer ID while said network port prepares to receive a packet; and if said packet will be forwarded, the corresponding TxDMA of network port will be selected to deliver said packet.

18. The said buffering management method as claimed in claim 16 or 17 in the patent range further includes carrying through a congestion control, and the said congestion control is needed to limit received packet, if all the total amount of non-reach value of said network port which waiting delivering packet has not reach the minimum threshold value is larger than or equal to a given predetermined value, as well as if the mount of other waiting delivering packet of said network port is larger than or equal to the minimum threshold value.

19. The said buffering management method as claimed in claim 16th or 17th item in patent range further includes carrying through a congestion control, and the said network port needs said congestion control to limit received packet when the waiting delivering packet amount of network port is larger than or equal to the maximum threshold value.

20. A kind of Ethernet switching buffering management method, the said Ethernet switching includes external memory with routing table and packet buffer, a buffer manager, and several network ports which include RxDMA and TxDMA, and the said buffering management method includes: in the initial state, the said packet buffer is constructed into a free list in the form of linked list, and a FreeHead register is used to indicate head index of the said packet buffer, and a FreeTail register is used to indicate tail index of the said packet buffer; when each said RxDMA interface sends receiving packet buffer requirement, the buffer index in the FreeHead register will be sent to the corresponding interface of said RxDMA; when each exchange happens, the said buffer index of said RxDMA interface will be added to the tail of delivering linked list of said forward network port, and claims that buffering manager has finished the exchange. When each said TxDMA sends delivering packet requirement, if the said delivering linked list is not empty, the said buffer index in head register of said delivering linked list will be delivered to the interface of said TxDMA; and when each delivering finished, the said buffer index of said TxDMA interface will be withdraw to said FreeTail register, and claims that buffering manager has finished withdrawing.

21. The said buffering management method as claimed in claim 20 in the patent range further includes carrying through a congestion control, and the said congestion control is needed to limit received packet, if all the total amount of non-reach value of said network port which packet has not reach the minimum threshold value is larger than or equal to a given predetermined value, as well as if the mount of other waiting delivering packet of said network port is larger than or equal to the minimum threshold value. When packets from other network port need to be forwarded to the said network port with congestion control, the said other network port will inform distal network port to stop delivering said packet through collision caused by delivering JAM packet, and the above control will not be rescinded until the congestion control condition disappears.

22. The said buffering management method as claimed in claim 20th item in patent range further includes carrying through a congestion control, and the said congestion control is needed to limit received packet, if the packet amount of any said network port is larger than or equal to the maximum threshold value. When packets from other network port need to be forwarded to the said network port with congestion control, the said other network port will inform distal network port to stop delivering said packet through collision caused by delivering JAM packet, and the above control will not be rescinded until the congestion control condition disappears.

Utility Model patent specification		
1. Name of the Utility Model patent	Chinese	
	English	Ethernet switching device with share memory structure and method of sharing the memory
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CPELP

Abstract

This patent specification provides an Ethernet switch which has a share memory structure to serve temporary packets access and routes record when switching packets between network ports. In addition, a buffer manager cooperated with buffer table are provided to manage the memory according to share memory methodology. The Ethernet switch consists of a memory device, a memory controller, a data switching controller and over two network ports. Where in these components, the memory device is used to access network packets and store routing, the memory controller which connects with memory device manages and controls network packets in memory. The

data switching controller connects with memory device too, which determines the path and routing learning that packets taken from senders to receivers. Each of the network ports is linked with the memory controller and the data switching controller.

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Ethernet switch with share memory structure

FIELD AND BACKGROUND OF THE INVENTION

The present invention is related to an Ethernet component, especially related to an Ethernet switch.

Ethernet is the most prevalent LAN technology in communication network market. The original structure for Ethernet was 10BASE5, which used a bus topology. Another was 10BASE2, a variation of 10BASE5, but largely reducing cost. The Ethernet 10BESE2 technology, as a bus topology network operating in 10 MHz clock frequency, using a coaxial cable for the bus, limited the maximum length of the connection to 200 meters. There were many disadvantages in both 10BASE5 and 10BASE2, such as the high cost of installation, low flexibility in network construction and incapability of utilizing existing premises distribution system. To overcome these drawbacks, 10BASE-T was proposed, with a star topology using twisted-pair cooper wire to build the network.

With increasingly large scale of LAN and excessive amount of data transmitting on it, performance of Ethernet will decline when connecting more nodes. A high-speed Ethernet, working on higher clock frequency, is suggested to meet the requirement of large scale LAN or high-speed data terminals. With a working frequency of 100MHz, this high-speed Ethernet can improve the performance of 10BASE. It defines a MII (Media Independent Interface). Network nodes can connect to the network through MII by twisted-pair copper wire or fiber cable. 100BASE-TX, 100BASE-T4 and 100BASE-FX are networks provided according to the above description.

10BASE5, 10BASE2, 10BASE-T, 100BASE-TX, 100BASE-T4 or 100BASE-FX is essentially a kind of share bandwidth network systems. All the nodes in network share the bandwidth. The bandwidth of 10BASE is 10MHz, and the 100BASE's is 100MHz. As the connected nodes exceed some threshold value, performance of system reaches saturation point. Thus, a segmenting methodology is presented to improve performance of Ethernet. The methodology, different from which accelerates working frequency, segments network into several sub-networks. Because every segment belongs to a different collision domain, the nodes connected to different sub-network don't share the bandwidth of others. For example, in a 100BASE LAN with 100 nodes, the share bandwidth of a node in the undivided LAN is 1MHz. However, if the LAN is divided into 2 segments, the share bandwidth of a node will be

2MHz. A LAN that has Ethernet protocol LAN segment is called a switched Ethernet. Packets belong to different segments are transmitted though Ethernet switches. The Ethernet switches are designed to switch packets between different segments. A packet in one segment will be forward to another segment, but the packet will not be switched if the source and destination are in the same segment. These common techniques are all exposed in USA patent number 5274631, 5491694, and 5588151.

Figure 1 shows the circuit of an Ethernet switch with a distribution memory structure.

Please refer to Figure 1, a common Ethernet switch consists of at least one switching IC 10 and multiple port ICs 11a, 11b, 11c. The switching IC controls data transfer between ports. There is a memory in each port IC, e.g., port IC 11a has a built-in memory 12a, offering functions of packets switching and access. Under this switching structure, as shown in Figure 1, data must be first stored in memory 12a when transmitting from port 13a to port 13c, then data are transferred to memory 12c. As a result, the memory size is determined when designing a port IC. However, any port of a switch can connect with different specific LANs, such as 10BASE5, 10BASE2, 10BASE-T, 100BASE-TX, 100BASE-T4 or 100BASE-FX. Therefore, it is necessary a large memory for fitting into different LANs. This causes a waste of memory. Another disadvantage is that the twice transmission of data which affects the performance of network switch.

As the problems exposed above, one purpose of the invention is to present a connection between 10BASE network and 100BASE network, extending the old system to a new one.

Another purpose is to present an Ethernet switch with a share memory structure, saving memory needed.

Final purpose of the invention is to reveal the method to implement the Ethernet switch described above, including method for share memory, a pool for packet buffer and share access, a solution for packet buffer pool congestion and a means for packet switch.

According to the purposes above, an Ethernet switch with share memory structure is proposed to selectively transmit network packets. The equipment consists of a memory device, a memory controller, a data switching controller and over two network ports. Among these components, the memory device is used to access network packets and store routing, the memory controller which connects with memory device manages and controls network packets in memory. The data switching controller connects with memory device too, which determines the path that packets taken from senders to receivers. Each of the network ports is linked with memory controller and

data switching controller.

According to the purposes above, an Ethernet switch with share memory structure is proposed to selectively transmit network packets. The equipment consists of a routing table, a packet buffer, a share memory access control, a data switching controller, over two network ports, a buffer manager, and a buffer table. Where in, the share memory access control connects with the routing table and the packet buffer, provides functions like arbitrating, data multiplex, address and command instruction. The data switching controller connects with share memory access control is responsible for routing table initialization, arbitrating, aging, and route learning and determination. Each network port respectively connects with share memory controller and data switching controller. The buffer manager connects with every network port. The buffer table connects with buffer manager. The routing table stores packet routing by share memory access control. The packet buffer accepts the access of every port packet by share memory access control. The buffer table records the state of use of the packet buffer through every port and share memory access control. The buffer manager manages packet buffer based on aware of the use state of the packet buffer by every port and the share memory access control.

One preferred implementation, according to this invention, is that the memory device should include a routing table and a packet buffer. The routing table stores the routing of the data switching controller by the connected memory controller. The packet buffer receives access of packets by the connected memory controller, too.

One preferred implementation, according to this invention, is that the memory controller should include an external memory interface and a memory manager. The external memory interface controls the access of data in memory by the connected memory device, data switching controller and every network port. The memory manager which connects with every network port manages the memory through external memory interface.

Another preferred implementation, according to this invention, is that the memory manager should include a buffer table and a buffer manager. The buffer table records the use state of memory through each network port and external memory interface. The buffer manager, which connects with the buffer table, manages packet buffer based on awareness of the use state of the packet buffer.

The other preferred implementation, according to this invention, is that data switching controller should include a routing controller and a route learning controller. The routing controller determines the routing of packets from network ports. The route learning controller stores the packet routing in routing table determined by routing controller through memory controller.

One preferred implementation, according to this invention, is that the routing controller determines which port to switch according to the destination address of the received packet. Meanwhile, the route learning controller selects the corresponding port according to the source address of the received packet.

One more preferred implementation, according to this invention, is that the network ports should include an Ethernet communication protocol controller and a packet access controller. The Ethernet communication protocol controller accomplishes the function defined in IEEE 802.3 section 4. The packet access controller receives and transmits packets.

One preferred implementation, according to this invention, is that the Ethernet communication protocol controller should include a media independent interface, an reconciliation sub-layer and a media access control. Functions of the media access control involve receiving and transmitting, and comply with the standard in IEEE 802.3 section 4.

One preferred implementation, according to this invention, is that the packet buffer controller should include a RxDMA and a TxDMA. The RxDMA is used to receive network packets. The TxDMA is used to deliver packets.

A buffer management technique for Ethernet switch is suggested according to another purpose of this invention. The Ethernet switch consists of an external memory which contains a routing table, a buffer manager, and multiple network ports that everyone contains a buffer controller and a TxDMA. The buffer management technique is as follows: first, the external memory is segmented into multiple blocks, with each block assigned an ID associated with packet location in it. Second, buffer manager maintains a link list of these IDs and dynamically allocates an ID to each forward packet. Then, the buffer manager distributes the unused IDs to packet access controller. Finally, the buffer manager reclaims these IDs from TxDMA.

According to the invention, the present buffer management technique includes: Whenever a network port receives a packet, the packet controller requests a buffer ID. If the packet is forwarding, the corresponding TxDMA of the network port is selected to transmit the packet based on this ID.

According to the invention, the present buffer management technique includes congestion control. If the sum of network ports, of which the number of waiting packets haven't reached the minimum threshold value, is less than or equal to a pre-specified value, then other network ports, whose number of waiting packets larger than or equal to the minimum threshold value, need congestion control. They are restricted to receive packets.

According to the invention, the present buffer management technique includes

congestion control. Any network port needs congestion control if the number of waiting packets is larger than or equal to the maximum threshold value. If so, it will be restricted to receive packets.

A buffer management technique for Ethernet switch is suggested according to another purpose of this invention. The Ethernet switch consists of an external memory which contains a routing table, a buffer manager, and multiple network ports that everyone contains a buffer controller and a packet extractor. The buffer management technique is as follows: during the initial state, a Free-List is constructed from the packet buffer using the form of link list. A Free-Header register stores the header index of the packet buffer, and a Free-Tail register stores the tail index. When buffer controller issues the request of receiving packets, the index in Free-Header register is passed to it. Then the index is added to the tail of a transmitting link list of the network port when switching packets. After this is done, the buffer controller is notified with switching accomplishment. If the transmitting link list is not empty, the buffer index in the Free-Header register will be passed to TxDMA when the TxDMA issues a request of transmitting packets. After the transmission is finished, the buffer index will be reclaimed to Free-Tail register and the TxDMA will be acknowledged reclamation have been completed.

According to the invention, the present buffer management technique includes congestion control. If the sum of network ports, of which the number of waiting packets haven't reached the minimum threshold value, is less than or equal to a pre-specified value, then other network ports, whose number of waiting packets larger than or equal to the minimum threshold value need congestion control. They are restricted to receive packets. The buffer index in the Free-Header register will be no longer passed to the corresponding buffer controller until the conditions above disappear.

According to the invention, the present buffer management technique includes congestion control. Any network port needs congestion control if the number of waiting packets is larger than or equal to the maximum threshold value. If so, it will be restricted to receive packets. The buffer index in the Free-Header register will be no longer passed to the corresponding buffer controller until the conditions above disappear.

BRIEF DESCRIPTION OF THE DRAWINGS

For the sake of assessor's appreciation of the present invention's purpose, characteristics and advantages, detailed description of the invention will be given below when considered in connection with the accompanying drawings, wherein:

FIG. 1 shows the circuit of a common Ethernet switch with distribution memory;

FIG. 2 shows the circuit of the Ethernet switch with share memory based on the first implementation of the present invention;

FIG. 3 shows the circuit of the Ethernet switch based on the second implementation of the present invention;

FIG. 4 shows the circuit of the memory device based on the second implementation of the present invention;

FIG. 5 shows the circuit of the memory controller based on the second implementation of the present invention;

FIG. 6 shows the circuit of the memory manager based on the second implementation of the present invention;

FIG. 7 shows the circuit of the data switch controller based on the second implementation of the present invention;

FIG. 8 shows the circuit of the network port based on the second implementation of the present invention;

FIG. 9 shows the circuit of the Ethernet switch based on the third implementation of the present invention;

FIG. 10 shows the architecture of the buffer management based on the third implementation of the present invention;

FIG. 11 shows the architecture of the buffer management based on the fourth implementation of the present invention;

FIG. 12 shows the congestion control of the buffer manager based on the fifth implementation of the present invention;

Notation of figures are interpreted as follows:

10 : switching IC

11a, 11b, 11c : port IC

12a, 12b, 12c : memory

13a, 13c : network port

20 : switching controller

21 : memory

22a, 22b, 22c : Media Access Controller, MAC

23a, 23c : network port

30 : memory device

31 : memory controller

32 : data switching controller

33a, 33b : network port

40 : routing table
41 : packet buffer
50 : external memory interface
51 : memory manager
60 : buffer manager
61 : buffer table
70 : routing controller
71 : learning controller
80 : Ethernet communication protocol controller
81 : packet access control
82 : Media Independent Interface, MII
83 : reconciliation sub-layer
84 : MAC
85 : Receive Direct Memory Access, RxDMA
86 : Transmit Direct Memory Access, TxDMA
90 : routing table
91 : packet buffer
92 : share memory access control
93 : data switching controller
94 : buffer manager
95 : buffer table
96a, 96b : network port

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 2 depicts the circuit of the Ethernet switch with share memory structure according to the first implementation of the present invention.

Please refer to FIG. 2, the Ethernet switch includes at least a switching controller and multiple MAC 22a, 22b, 22c. The switching IC 20 with a share memory 21 controls data switching of network ports which belong to MAC. Given the switching architecture of the present invention, it is only necessary for data to pass through memory 21 when delivered from port 23a to 23c. That is, data are first stored in memory 21 through MAC 22a, then MAC 22c gets them from memory 21, as shown in FIG. 2. The memory 21 is shared by all the MACs so that it can be used efficiently, also cost is cut. In addition, a new means of packet switching springs by accessing the data of network ports directly in share memory 21.

FIG. 3 is the circuit of the Ethernet switch according to the second implementation of the present invention.

Refer to FIG. 3, the Ethernet switch based on the second implementation includes a memory device 30, a memory controller 31, a data switching controller 32, and multiple network ports, such as 33a, 33b. The memory device 30 is an external memory, offering the functionality of packets accessing and routing storage. The memory controller 31 manages and takes control of the packets in the memory device 30. The data switching controller 32 determines the routing and route learning of packets. The networks 33a, 33b comply with Ethernet communication protocol, such as the standard described in IEEE 802.3 section 4.

Refer to FIG. 3, the connections between components based on the second implementation are illustrated as follows: the memory controller connects to the memory device 30. The data switching controller 32 connects with the memory controller 31. The first network port 33a and 33b both connect with the memory controller 31 and the data switching controller 32.

FIG. 4 is the circuit of the memory device according to the second implementation of the present invention.

Please refer to FIG. 4, the memory device 30 includes a routing table 40 (or an address table) and a packet buffer 41. The routing table accesses the routing data of the data switching controller 32 by the connected memory controller 31. The packet buffer 41 receives accessing of packets of the first and second network port 33a, 33b by the connected memory controller 31.

FIG. 5 shows the circuit of the memory controller according to the second implementation of the present invention, and FIG. 6 shows the circuit of the memory manager with the same implementation.

As shown in FIG. 5, the memory controller 31 consists of an external memory interface 50 and a memory manager 51. The external memory interface 50, in connection with the memory device 30, data switching controller 32, and the first and the second network port 33a, 33b, takes control of data access in memory device 30. That is, the external memory interface acts as the interface between the above components and the memory device 30. As shown in FIG. 6, the memory manager 51, managing the memory device 30, includes a buffer manager 30 and a buffer table 61. The buffer table 61 records the use state of the memory device 30 by the network port 33a or 33b, and the external memory interface 50. The buffer manager 60 is aware of the state of buffer by the connected buffer table 61, and manages the packet buffer 41 via this information.

FIG. 7 is the circuit of the data switching controller according to the second implementation of the present invention.

As depicted in FIG. 7, the data switching controller 32 includes a routing

controller 70 and a learning controller 71. The routing controller 70 determines the delivery paths for each network port 33a, 33b. After a path is selected, the learning controller 71 stores it in the routing table of the memory device 30, via the memory controller 31. The routing controller 70 selects the corresponding network port depending on destination address of the received packet. The learning controller 71 selects the corresponding network port depending on source address of the received packet.

FIG. 8 is the circuit of the network port according to the second implementation of the present invention.

As shown in FIG. 8, any network port 33a, 33b includes an Ethernet communication controller 80 and a packet access control 81. The Ethernet communication controller 80 accomplishes the functionalities described in IEEE 802.3 section 4. It includes a MII 82, a reconciliation sub-layer 83 and a MAC 84. The packet access control 81 should include a RxDMA 85 and a TxDMA 86. The MAC 84 has the functionalities of receiving and transmitting, which comply with the standard in IEEE 802.3 section 4.

In succession, take a look at FIG. 9, an Ethernet switch will be given an explanation below, according to the third implementation of the present invention. FIG. 9 is the relevant circuit of the Ethernet switch.

As shown in FIG. 9, the Ethernet switch, according to the third implementation of the present invention, includes a routing table (or an address table) 90, a packet buffer 91, a share memory access control 92, a data switching control 93, a buffer manager 95, a buffer table 94, a first network port 96a, and a second network port 96b.

In FIG. 9, the share memory access control 92 is provided with the functionalities of arbitrating, data multiplexing, address, memory access commands, and so on. The tasks of the data switching control 93 involves initializing, arbitrating, aging of the routing table 90, and routing and learning of delivery paths. Other components in FIG. 9 are the same as in the second implementation, such as routing table 90, packet buffer 91, packet manager 94, buffer table 95, the first network port 96a, and the second network port 96b.

Next, the method of sharing memory in the Ethernet switch is explored. For a clear view of the method, details of the buffer manager and buffer table are given first below.

First, the buffer manager is described here. The external memory (for example, 512K or 256K byte) used by buffer manager can be segmented into 341 or 170 blocks (1.5K byte/block), and each block is assigned a buffer ID to represent the corresponding packet location in the external memory. Buffer IDs 0~21 are designated

for the routing table. The buffer manager maintains a linked list of buffer ID and dynamically allocates a buffer ID to each forward packet. The buffer manager together with the interfaces of RxDMA and TxDMA of each network port, assign and allocate free buffer IDs to RxDMA, and reclaim them from TxDMA. Whenever a packet is received, a buffer ID is requested by the RxDMA. If the packet is forward, the TxDMA will transmit it according to the packet's buffer ID.

The buffer manager also executes congestion control. If the incoming packets are more than the outgoing's, the number of free buffer IDs available will decrease rapidly. When a network port uses up all reserved free buffer IDs, the buffer manager will emit a low-control alarm signal.

Following the explanation of the buffer table will be given. The buffer table is built in a chip. It's a linked list implemented by free buffer IDs and packet buffer IDs. Each network port has its own linked list of buffer IDs, which form a transmitting sequence. A linked list of free buffer IDs can be shared by two network ports.

Next, the method of sharing memory in the Ethernet switch is illustrated with the accompany FIG. 10, which shows the architecture of the buffer manager on the basis of the third implementation.

As shown in FIG. 10, the free buffer IDs are combined and organized into a linked list. With a FreeHead and a FreeTail register, the head buffer ID, the tail buffer ID, and the connected relationship in initial state can be pointed out. When RxDMA issues FreeRxReqB, the buffer ID that the FreeHead register points to is assigned to RxDMA. FreeRxData and FreeRxWrite represent the data of buffer IDs and the written signal, respectively. When Filtering/Forwarding of a packet is finished, SwitchValidB of the RxDMA denoting packet forwarding, the buffer manager will supplement the Tx-List with the SwitchBuf according dependent on SwitchDp. When TxDMA issues RxTxInRdyB, and the Tx-List is not empty, the head buffer ID of Tx-List will be obtained and transferred by TxDMA. RxTxData and RxTxWrite represent the data of buffer IDs and the written signal. When a packet is transmitted, unused buffer IDs will be reclaimed to the tail of the Free-List. If the TxFreeRdy request is admitted by TxDMA, TxFree will be sent to FreeTail.

Next, the method of buffer management of the Ethernet switch is illustrated with the accompany FIG. 11, which shows the architecture of the buffer manager on the basis of the fourth implementation. The method of buffer management based on the fourth implementation of the present invention is described as follows:

(1) During the initial state, Free-List will be constructed in the form pf linked list. A FreeHead register is used to point to the head index of the packet buffer, and a FreeTail register points to the tail index.

(2) When a Rx-interface issues FreeRxReqB, the buffer index in FreeHead register will be sent to Rx-interface via FreeRxData and FreeRxWrite.

(3) For each SwitchValidB, the buffer index in SwitchBuf is appended to the tail of TxLink of the network port. SwitchDp indicates the network port. SwitchBufq points out the buffer ID. Q9 gives out the buffer IDs sent to each network port. EndSwitchB notifies the buffer manager when switching is accomplished.

(4) For each rxTxInRdyB, if TxLink is not empty, the buffer index (or the buffer ID) of the TxLink in the Head register is sent to Tx-interface via RxTxData and RxTxWrite.

(5) For each TxFreeRdy, the buffer index sent by Tx-interface to TxFree will be reclaimed to FreeTail. EndTxFree informs the buffer manager when reclamation finished.

The congestion control will be explained follow. The buffer manager executes congestion control when network ports work in half duplex mode. Of any network port, if the number of packets waiting for transmission exceeds a pre-specified threshold value, it will issue the FloodCrtl signal. If the number of waiting packets of some network port exceeds the pre-specified threshold value, whereas another port is receiving some packets which need to be forwarding to the previous port, there will be a collision between the JAM form packet from another port and the incoming packet. This collision phenomenon causes the remote network port stopping the transmission of packets. Thus, buffer overflow and packet loss can be avoided.

The total number given by the maximum buffer ID depends on line speed of each network port: (where in, 22 buffer IDs must be given to the 32K byte routing table).

Under the circumstance of using 512K byte memory, if all the pair of network ports operating in 10Mbps mode, the congestion control threshold value will be set to 155. If one works in 10Mbps, the other works in 100Mbps, then threshold value of the port working in 10Mbps will be set to 278, whereas, the port of 100Mbps, will be set to 32.

(1) 512K byte memory device, the threshold value table of congestion control

Network working mode	Threshold values of congestion control
10Mbps/10Mbps	155/155
100Mbps/100Mbps	155/155
10Mbps/100Mbps	278/32
100Mbps/10Mbps	32/278

(2) 216K byte memory device, the threshold value table of congestion control

Network working mode	Threshold values of congestion control
10Mbps/10Mbps	69/69
100Mbps/100Mbps	69/69
10Mbps/100Mbps	122/16
100Mbps/10Mbps	122/16

The above example is about two network ports. The principle of setting the maximum value of the buffer ID for each network port is that low line speed network ports are assigned larger threshold values, and high line speed's with smaller values. As a result, congestion of some specific network port, such as a port with low line speed, will be avoided.

The congestion control of the buffer manager includes the maximum and minimum control of the threshold value. Please refer to FIG. 12, which is the congestion control of the buffer manager according to the fifth implementation of the present invention.

As showed in FIG. 12, Port i represents the ith network port. TxLinkCnt[i] is the number of packets waiting for transmission. MaxCtrl[i] is the maximum permitted threshold value for waiting packets. MinCtrl[i] is the minimum permitted threshold value for waiting packets.

When executing minimum control, if the total number of network ports, which all the packets waiting for transmission haven't reached minimum threshold value, is larger than or equal to some pre-specified value, other network ports, whose number of packets waiting for transmission is larger than or equal to minimum threshold value, need congestion control, as the equation (1) in FIG. 12. When executing maximum control, any network port, whose number of packets is larger than or equal to the maximum threshold value, needs congestion control, as the equation (2) in FIG. 12.

As can be known from the above implementations, the advantages of the present invention are:

(1) The functionalities of 10BASE and 100BASE can be connected to extend the old system into a new one.

(2) With share memory structure, the memory of the switch can be saved and the performance can be improved a lot.

(3) The congestion of the buffer manager, not only avoids overflow of buffer, but also avoids the loss of packets.

The Ethernet switch described above is only a preferred embodiment of the present invention, not a confinement of employment. Obviously, numerous equivalent modifications or variations of the present invention are possible in light of the above

teachings. It is therefore to be understood that they are all within the scope of the practical new type patent.

PATENT RANGE:

1. A kind of Ethernet switching device with share memory structure, which is used to deliver network packet selectively, the said device includes:

A memory device which provides accessing network packet, and store network routing data;

A memory controller coupled to the said memory device is used to manage and control network packet in the said memory device;

A data switching controller coupled to the said memory device is used to control the routing and learning of network packet routing;

And two network ports which are coupled to said memory controller and data switching controller.

2. The said Ethernet switching device as claimed in claim 1 in the patent range, wherein the said memory device further includes:

A routing table coupled to the said memory controller, which stores the routing table data of the said data switching controller through the said memory controller;

And a packet buffer coupled to the said memory controller, which allows packet access of every said network port through the said memory controller.

3. The said Ethernet switching device as claimed in claim 1 or 2 in the patent range, wherein the said memory controller further includes:

An external memory interface coupled to the said memory device, said data switching controller, and every said network port respectively, which is used to control the data access of the said memory device;

And a memory manager coupled to every said network port respectively, which manager the said memory device through the said external memory interface.

4. The said Ethernet switching device as claimed in claim 3 in the patent range, wherein the said memory manager further includes:

A buffer table records the usage state of the said memory device through every said network port and said external memory interface;

And a buffer manager coupled to the said buffer table, which managers the said

packet buffer according to the obtained usage state of the said packet buffer.

5. The said Ethernet switching device as claimed in claim 1st or 2nd item in patent range, in which, the said data switching controller further includes:

A routing controller which is used to select the packet routing of every said network port;

And a learning controller which is used to store the packet routing selected by the said routing controller into the routing table of the said memory device through the said memory controller.

6. The said Ethernet switching device as claimed in claim 5 in the patent range, wherein the said routing controller should route the corresponding network port selectively according to the destination address of received packet.

7. The said Ethernet switching device as claimed in claim 5 in the patent range, wherein the said learning controller should route the corresponding network port selectively according to the source address of received packet.

8. The said Ethernet switching device as claimed in claim 1 or 2 in the patent range, wherein the said network port further includes:

An Ethernet communication protocol controller which mainly accomplishes the function regulated by IEEE 802.3 section 4;

And a network packet data access controller which is used to receive and deliver network packet.

9. The said Ethernet switching device as claimed in claim 8th item in patent range, in which, the said Ethernet communication protocol controller further includes:

A MII;

A reconciliation sub-layer;

And a MAC that has receiving and delivering function which are accord with IEEE 802.3 section 4.

10. The said Ethernet switching device as claimed in claim 8 in the patent range, wherein the said network packet data access controller further includes:

An RxDMA which is used to receive network packet;

And TxDMA which is used to deliver network packet.

11. A kind of Ethernet switching device with share memory structure, which is used to deliver network packet selectively, the said device includes:

A routing table;

A packet buffer;

A share memory access controller coupled to the said routing table and said packet buffer respectively, which has arbitrating, data multiplexing, address, and commands function;

A data switching controller coupled to the said share memory access controller, which has initializing, arbitrating, aging routing table, routing and learning function;

More than two network ports, and every said network port is coupled to the said share memory access controller and said data switching controller respectively;

A buffer manager coupled to every said network port;

And a buffer table coupled to said buffer manager;

In which, the said routing table stores the routing data of the said data switching controller through the said share memory access controller; the packet buffer accepts packet accessing of every said network port through the said share memory access controller; the said buffer table records the usage state of the said packet buffer through every said network port and share memory access controller; and the said buffer manager managers the said packet buffer according to the obtained usage state of the said packet buffer through every said network port and said share memory access controller.

12. The said Ethernet switching device as claimed in claim 11 in the patent range, where the said network port further includes:

An Ethernet communication protocol controller which mainly accomplishes the function regulated by IEEE 802.3 section 4;

And a network packet data access controller which is used to receive and deliver network packet.

13. The said Ethernet switching device as claimed in claim 12 in the patent range, wherein the said Ethernet communication protocol controller further includes:

A MII;

A reconciliation sub-layer;

And a MAC that has receiving and delivering function which are accord with IEEE 802.3 section 4.

14. The said Ethernet switching device as claimed in claim 12 in the patent range,

wherein the said network packet data access controller further includes:

An RxDMA which is used to receive network packet;

And TxDMA which is used to deliver network packet.

15. A kind of Ethernet switching device which is used to deliver network packet selectively, the said device includes:

Multiple MAC which is used to receive and deliver network packet;

And a switching controller coupled to every said network port respectively, which has a share memory to control the ports of every MAC.

16. A kind of Ethernet switching buffering management method, the said Ethernet switching includes external memory with routing table, a buffer manager, and several network ports which include RxDMA and TxDMA, and the said buffering management method includes:

Dividing the said external memory into several blocks, and assigning a buffer ID to every said block to present the relative packet position of external memory;

The said buffer manager maintains the linked list of the said buffer ID, and assigns the said buffer ID dynamically to every forward packet;

The said buffer manager assigns free buffer ID to said RxDMA;

And the said buffer manager withdraws said buffer ID from TxDMA.

17. The said buffering management method as claimed in claim 16 in the patent range further includes:

The said RxDMA will need a buffer ID while said network port prepares to receive a packet;

And if said packet will be forwarded, the corresponding TxDMA of network port will be selected to deliver said packet.

18. The said buffering management method as claimed in claim 16 or 17 in the patent range further includes carrying through a congestion control, and the said congestion control is needed to limit received packet, if all the total amount of non-reach value of said network port which waiting delivering packet has not reach the minimum threshold value is larger than or equal to a given predetermined value, as well as if the mount of other waiting delivering packet of said network port is larger than or equal to the minimum threshold value.

19. The said buffering management method as claimed in claim 16 or 17 in the

patent range further includes carrying through a congestion control, and the said network port needs said congestion control to limit received packet when the waiting delivering packet amount of network port is larger than or equal to the maximum threshold value.

20. A kind of Ethernet switching buffering management method, the said Ethernet switching includes external memory with routing table and packet buffer, a buffer manager, and several network ports which include RxDMA and TxDMA, and the said buffering management method includes:

In the initial state, the said packet buffer is constructed into a free list in the form of linked list, and a FreeHead register is used to indicate head index of the said packet buffer, and a FreeTail register is used to indicate tail index of the said packet buffer;

When each said RxDMA interface sends receiving packet buffer requirement, the buffer index in the FreeHead register will be sent to the corresponding interface of said RxDMA;

When each exchange happens, the said buffer index of said RxDMA interface will be added to the tail of delivering linked list of said forward network port, and claims that buffering manager has finished the exchange.

When each said TxDMA sends delivering packet requirement, if the said delivering linked list is not empty, the said buffer index in head register of said delivering linked list will be delivered to the interface of said TxDMA;

And when each delivering finished, the said buffer index of said TxDMA interface will be withdraw to said FreeTail register, and claims that buffering manager has finished withdrawing.

21. The said buffering management method as claimed in claim 20 in the patent range further includes carrying through a congestion control, and the said congestion control is needed to limit received packet, if all the total amount of non-reach value of said network port which packet has not reach the minimum threshold value is larger than or equal to a given predetermined value, as well as if the mount of other waiting delivering packet of said network port is larger than or equal to the minimum threshold value. When packets from other network port need to be forwarded to the said network port with congestion control, the said other network port will inform distal network port to stop delivering said packet through collision caused by delivering JAM packet, and the above control will not be rescinded until the congestion control condition disappears.

22. The said buffering management method as claimed in claim 20 in the patent range further includes carrying through a congestion control, and the said congestion control is needed to limit received packet, if the packet amount of any said network port is larger than or equal to the maximum threshold value. When packets from other network port need to be forwarded to the said network port with congestion control, the said other network port will inform distal network port to stop delivering said packet through collision caused by delivering JAM packet, and the above control will not be rescinded until the congestion control condition disappears.

10：交换积体电路 switching IC
11a，11b，11c：埠积体电路 port IC
12a，12b，12c：记忆体 memory
13a，13c：网路埠 network port
20：交换控制器 switching controller
21：记忆体 memory
22a，22b，22c：介质存取控制 MAC(media access control)
23a，23c：网路埠 network port
30：记忆体装置 memory device
31：记忆体控制器 memory controller
32：资料交换控制器 data switching controller
33a，33b：网路介面埠 network port
40：传递路径储存记忆体 routing table
41：网路封包储存记忆体 packet buffer
50：记忆体介面控制装置 external memory interface
51：记忆体管理装置 memory manager
60：缓冲器管理装置 buffer manager
61：缓冲器使用状态记录装置 buffer table
70：传递路径选定控制器 routing controller
71：传递路径学习控制器 learning controller
80：乙太网路通讯协定控制器 Ethernet communication protocol controller
81：网路封包资料存取控制器 network packet data access controller
82：介质不相关介面 MII
83：调和附属层 reconciliation sub-layer
84：介质存取控制器 MAC
85：网路接收封包资料储存控制器 RxDMA(receive direct memory access)
86：网路传送封包资料撷取控制器 TxDMA(transmit direct memory access)
90：传递路径储存记忆体 routing table
91：网路封包储存记忆体 packet buffer
92：共享记忆体存取控制器 share memory access controller
92a：仲裁器 arbitrator

92b：资料多工器 data multiplexer
92c：定址器 addressing device
92d：存取命令控制器 command controller
93：资料交换控制器 data switching controller
93a：传递路径储存记忆体初始化控制器 initialization controller
93b：仲裁器 arbitrator
93c：传递路径储存记忆体老化控制器 aging controller
93d：网路传递路径选定控制器 routing controller
93e：网路传递路径学习控制器 learning controller
94：缓冲器使用状态记录装置 buffer table
95：缓冲器管理装置 buffer manager
注：图94，95和原文（发明说明12）不符，正好相反
96a：第一网路介面埠 the first network port
96b：第二网路介面埠 the second network port